**SILIGURI INSTITUTE OF TECHNOLOGY**
**COMPUTER SCIENCE & ENGINEERING**

# COURSE FILE

## 1ST SEM, 2ND YEAR, 2020

**SEC – B**

**PAPER DESCRIPTION : Computer Organization**

**PAPER CODE : PCC CS 302 & PCC CS 392**

# Course File

**Course Title:** Computer Organization

**Code :** PCC CS302 & PCC CS392

**Semester:-** 1st **Year:-** 2nd

**Name of the Faculty:** Prof. Jayashree Singha

**Internet Homepage:**

**E-mail :** jaysin31m85@gmail.com

| Lecture | | | Practical |
|---|---|---|---|
| **Monday**<br>11:40 AM – 12:30 PM | **Wednesday**<br>10: 50 AM – 11:40 AM | **Thursday**<br>10: 50 AM – 11:40 AM | **Tuesday**<br>2:10 PM – 4:40 PM (B1)<br>**Thursday**<br>2:10 PM – 4:40 PM (B2) |

| **Hours for meeting students:** |
|---|
| **Monday to Friday 4.40 PM -5.30 PM** |

## i) Course Objective

**Students will be able to have a comprehensive understanding of the basic structure and operation of a digital computer.**

## ii) Course Outcomes

i. After completion of this course the students are expected to be able to demonstrate following knowledge, skills and attitudes.

The student will be able to:

| | | Target |
|---|---|---|
| **PCC CS302.1** | Describe Stored Program Digital Computer System. [B.T. LEVEL* 2] | 60% Marks |
| **PCC CS302.2** | Identify & apply appropriate procedures and algorithms of Computer Arithmetic. [B.T. LEVEL*3] | 60% Marks |
| **PCC CS302.3** | Explain different aspects of Central Processing Unit (CPU). [B.T. LEVEL* 2] | 60% Marks |

| | | |
|---|---|---|
| **PCC CS302.4** | Understand the fundamentals of Memory Unit and illustrate memory operations. [B.T. LEVEL* 3] | 60% Marks |
| **PCC CS302.5** | Explain models of I/O operations & the I/O subsystems. [B.T. LEVEL* 2] | 60% Marks |
| **PCC CS302.6** | Identify the micro-instructions and basics of Computer Architecture. [B.T. LEVEL* 2] | 60% Marks |

ii. Once the student has successfully complete this course, he/she must be able to answer the following questions or perform / demonstrate the following:

| Sl. | Question | CO |
|---|---|---|
| **1.** | **Describe** the major components of a digital computer with a suitable block diagram. | 1 |
| **2.** | **Explain** Booth's algorithm for multiplication of signed 2's complement number in flow chart. | 2 |
| **3.** | **Explain** IEEE 754 standard format for floating point representation in single precision. | 2 |
| **4.** | **Compare** parallel adder with serial adder. | 3 |
| **5.** | **Explain** the memory hierarchy pyramid with the relationship of cost, speed and capacity. | 4 |
| **6.** | **Explain** the difference between full associative and direct mapped cache mapping approaches. | 4 |
| **7.** | **Explain** the Write-through and Write-back mechanism. | 4 |
| **8.** | **Explain** the concept of hand shaking in IO operation. | 5 |
| **9.** | **Compare** the difference between three, two, one and zero address instructions. | 6 |
| **10.** | **Compare** RISC and CISC architecture. | 6 |

## iii) Topic/Unit/Chapter Layout

| Chapter No. | Topic/Unit/Chapter | Lecture Hours | Tutorials | Laboratory hours |
|---|---|---|---|---|
| **Chapter** - 1 | Fundamentals of Computers | 3 HRS | - | -- |
| **Chapter** – 2 | Data Representation and computer Arithmetic | 7 HRS | 5 | 16 HRS |
| **Chapter** – 3 | Micro-operations and Design of ALU | 5 HRS | 1 | 6 HRS |
| **Chapter** – 4 | Memory Organization | 9 HRS | 3 | 6 HRS |

| | | | | |
|---|---|---|---|---|
| **Chapter** – 5 | Computer Instruction Sets | 6 HRS | 1 | |
| **Chapter** – 6 | Design of Control Unit | 1 HRS | | |
| **Chapter** – 7 | Input Output Organization | 4 HRS | | |
| **Chapter** – 8 | Parallel Processing | 4 HRS | | |
| Total | | 39 HRS | 10 HRS | 28 HRS |

## iv)Textbooks


1. Mano, M.M., "Computer System Architecture", PHI.
2. Behrooz Parhami "Computer Architecture", Oxford University Press


## Reference books :


1. Hayes J. P., "Computer Architecture & Organisation", McGraw Hill,
2. Hamacher, "Computer Organisation", McGraw Hill,
3. N. senthil Kumar, M. Saravanan, S. Jeevananthan, "Microprocessors and Microcontrollers" OUP
4. Chaudhuri P. Pal, "Computer Organisation & Design", PHI,
5. P N Basu- "Computer Organization & Architecture" , Vikas Pub


## 2) Laboratory

| Expt. No. | Experiment Name | Schedule | Marks |
|---|---|---|---|
| P1 | Familiarization with IC chips:<br>a) 4:1 MUX,<br>b) 16:1 MUX<br>c) Decoder<br>d) Encoder<br>e) Comparator<br><br>Truth table verification and clarification from data-book. | 7 HRS | 15 |
| P2 | Design of Adder/Subtractor composite unit | 2 HRS | 4 |
| P3 | Design of BCD Adder | 2 HRS | 4 |
| P4 | Design of Carry Look-Ahead Adder | 3 HRS | 2 |
| P5 | Use a multiplexer unit to design a composite ALU | 3 HRS | 4 |
| P6 | Use ALU chip for multi-bit arithmetic operation | 3 HRS | 3 |
| P7 | Implement read/write operation using RAM IC | 3 HRS | 4 |

| | | | |
|---|---|---|---|
| P8 | Cascade two ICs for<br>a) vertical expansion<br>b) horizontal expansion | 3 HRS | 4 |
| | | Total | 40 |
| | | University Exams | 60 |

## (v) Evaluation Scheme

### 1) Theory

| Evaluation Criteria | Marks |
|---|---|
| Continuous Assessment | 25 |
| Attendance | 5 |
| University Exam/External Exam | 70 |
| Total | 100 |

* The Internal assessment will be determined through the continuous assessment (CA) which is needed to be submitted 4 times in a semester based on performance of the students assessed as per academic calendar published by the University. The 4 no's of CAs will be based on test/ viva/ quiz/ presentation/seminar/ GD etc. out of which 2 no's preferably would be tests.

### Schedule for Continuous Assessment (CA):

| CA Description | Schedule |
|---|---|
| Quiz – 1 | As per Institute Academic Calendar |
| 1st Internal Examination | |
| Quiz – 2 | |
| Assignment | |
| 2nd Internal Examination | |

### Course target attainment levels:

| Attainment Level | Inference | Marks |
|---|---|---|
| Attainment Level 1 | 50% of the students have attained more than the target level of that CO | 1 |

| | | |
|---|---|---|
| Attainment Level 2 | 60% of the students have attained more than the target level of that CO | 2 |
| Attainment Level 3 | 70% of the students have attained more than the target level of that CO | 3 |

**Course Target for the university examination = 60% of the students will get "A" Grade**

Target has been set on the basis of last year's performance / result by the students, student quality this year and difficulty level of the course.

**University Grading System:**

| Grade | Marks |
|---|---|
| O | 90% and above |
| E | 80 – 89.9% |
| A | 70 – 79.9% |
| B | 60 – 69.9% |
| C | 50 – 59.9% |
| D | 40 – 49.9% |
| F | Below 40% |

## (vi) Mapping of Course Outcomes and Program Outcomes:

| Course Outcomes | Program Outcomes (PO's) | | | | | | | | | | | | PSOs | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| PCC CS302.1 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | - | - | 2 |
| PCC CS302.2 | 2 | 3 | 3 | 2 | - | - | - | - | 3 | 1 | - | - | 1 | 2 |
| PCC CS302.3 | 2 | 3 | 3 | 2 | - | - | - | - | 3 | 1 | - | - | 1 | 3 |
| PCC CS302.4 | 2 | 3 | 3 | 2 | - | - | - | - | 3 | 1 | - | - | 1 | 3 |
| PCC CS302.5 | 2 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | - | 3 |
| PCC CS302.6 | 2 | 2 | 2 | 1 | - | - | - | - | - | - | - | - | - | 2 |
| PCC CS302 | **2** | **3** | **3** | **2** | **-** | **-** | **-** | **-** | **3** | **1** | **-** | **-** | **1** | **3** |

**1** = courses in which the student will be exposed to a topic (BT level 1- 2)
**2** = courses in which students will gain competency in that area (BT level 3-4)
**3**= courses in which students will master that skill (BT level 5-6)

## (vii) Delivery Methodology

| Outcome | Method | Supporting Tools | Demonstration |
|---|---|---|---|
| PCC CS302.1 | Structured (partially supervised Whole Class- grouping) | Google class Room, Gmeet Lecture Notes, PPT | Introduction to Von-Neumann and Harvard architecture. |
| PCC CS302.2 | Structured (partially supervised Whole Class- grouping) | Google class Room, Gmeet Lecture Notes, PPT | Representation of floating point numbers and solving computer arithmetic using algorithms. |
| PCC CS302.3 | Structured (partially supervised Whole Class- grouping and independent work) | Google class Room, Gmeet Lecture Notes, PPT | Familiarization with the design of CPU. |
| PCC CS302.4 | Structured (partially supervised Whole Class- grouping) | Google class Room, Gmeet Lecture Notes, PPT | Explanation of memory unit and implementation of memory operation. |
| PCC CS302.5 | Structured (partially supervised Whole Class- grouping) | Google class Room, Gmeet Lecture Notes, PPT | Demonstration of the I/O unit of computer. |
| PCC CS302.6 | Structured (partially supervised Whole Class- grouping) | Google class Room, Gmeet Lecture Notes, PPT | Identification of basic computer instructions and micro-operations. |

## (viii) Assessment Methodology

| Outcome | Assessment Tool |
|---|---|
| PCC CS302.1 | Internal Test, Quiz, Assignment, University Exam |
| PCC CS302.2 | |
| PCC CS302.3 | |
| PCC CS302.4 | |
| PCC CS302.5 | |

## (ix) A. Weekly Lesson Plan

| CHAPTER / UNIT | Topic Description (to be quoted from syllabus) | No. of Lectures | Plan Date(s) | Execution Date(s) | Homework/ Assignment/ Quiz |
|---|---|---|---|---|---|
| I | **Fundamentals of Computers** | | | | |
| Unit-I | Concept of basic components of a digital computer, Basic concept of Fundamentals & Program structures. Role of operating systems and compiler/assembler. | 1 | 16.7.20 | | |
| | Stored program concept, Von-Neumann architecture | | 20.7.20 | | |
| | Basic number systems, Binary Arithmetic (Add, Sub, Mul, Div), Logic Gates, Boolean Algebra, BCD Addition, Binary Subtraction, 2's complement addition. | 1 | 22.7.20 | | |
| | Concepts of Combinational Circuits: MUX, DEMUX, Decoder, Encoder, Sequential Circuit (Flip- Flop). | 1 | 23.7.20 | | |
| | **Assessment on this CHAPTER** | -- | | | Quiz |
| II | **Data Representation and Computer Arithmetic** | | | | |

| | | | | | |
|---|---|---|---|---|---|
| Unit-III | Signed representation of Fixed point numbers. Arithmetic overflow. | 1 | 27.7.20 | | |
| | Floating point representation of numbers (IEEE 754 standard), Overflow and underflow of floating point numbers. | 1 | 29.7.20 | | Homework |
| | Fixed point multiplication -Booth's algorithm. | 1 | 30.7.20 | | Homework |
| | Fixed point division - Restoring algorithms. | 1 | 3.8.20 | | Homework |
| | Fixed point division -Non-restoring Algorithm | 1 | 5.8.20 | | Homework |
| | **Assessment on this CHAPTER** | -- | | | Assignment |
| **III** | **Micro-operations and Design of ALU** | | | | |
| Unit-III | HA, FA, serial and parallel adders, Design of adders – Ripple carry adder, | 1 | 6.8.20 | | |
| | Carry look-ahead principles. | 1 | 10.8.20 | | |
| | Adder-Subtractor Unit, Binary Incrementer Unit, Decrementer Unit, | 1 | 12.8.20 | | |
| | Computer Registers. Bus (Data/ Address/ Control) | 1 | 13.8.20 | | |
| | Common Bus System | 1 | 17.8.20 | | |
| | Design of the Arithmetic and logic Unit of ALU | | 19.8.20 | | |
| | Design of the shift Unit of ALU, Design of one stage of ALU | | 20.8.20 | | |
| | **Assessment on this CHAPTER** | -- | | | Quiz |
| **IV** | **Memory Organization** | | | | |
| Unit-IV | Memory Organization: Memory Hierarchy, Main Memory architecture, Implementation of CPU-memory interfacing, RAM and ROM chips. | 1 | 24.8.20 | | |
| | Types of RAM and ROM chips, classification of Secondary memory | 1 | 26.8.20 | | |
| | Memory address map | 1 | 27.8.20 | | Homework |
| | Associative memory/ CAM: Cache memory | 1 | 31.8.20 | | |
| | Memory read/write cycle, avg. access time calculation | 1 | 2.9.20 | | |
| | Cache mapping techniques | 1 | 3.9.20 | | |
| | Cache mapping techniques | 1 | 7.9.20 | | |
| | Replacement methods, cache write | 1 | 9.9.20 | | |

| | | | | | |
|---|---|---|---|---|---|
| | methods, techniques to reduce cache miss | | | | |
| | Virtual memory | 1 | 10.9.20 | | |
| | **Assessment on this CHAPTER** | | | | Quiz/ Assignment |
| **V** | **Computer Instruction Sets** | | | | |
| **Unit-V** | Basic Instruction format, Immediate, Direct address, Indirect address, Effective addresses. Instruction Formats : Memory/ Register/Input-Output reference. | 1 | 14.9.20 | | |
| | Types of Instruction: Data Transfer/ Data Manipulation/ Program Control | 1 | 16.9.20 | | |
| | Zero/One/Two/Three address instructions, RISC instructions. | 1 | 21.9.20 | | Homework |
| | Introduction to RISC architectures, RISC vs. CISC architectures. | 1 | 24.9.20 | | |
| | Fetch, decode and execute cycle | 1 | 28.9.20 | | |
| | **Assessment on this CHAPTER** | | | | Quiz/ Assignment |
| **VI** | **Design of Control Unit** | | | | |
| **Unit-VI** | Design of control unit (CU) – hardwired and micro-programmed control | 1 | 1.10.20 | | |
| | **Assessment on this CHAPTER** | -- | | | Quiz |
| **VII** | **Input Output Organization** | | | | |
| **Unit-VIII** | Synchronous and Asynchronous data transfer, I/O operations - Concept of handshaking I/O | 1 | 5.10.20 | | |
| | Modes of data transfer: programmed I/O, interrupt driven I/O. | 1 | 7.10.20 | | |
| | Priority interrupt , Daisy chain, Polling | 1 | 8.10.20 | | |
| | Direct Memory Access (DMA) | 1 | 12.10.20 | | |
| | **Assessment on this CHAPTER** | -- | | | Quiz |
| **VIII** | **Parallel Processing** | | | | |
| **Unit-VIII** | Pipelining | 1 | 14.10.20 | | |
| | Hazards | 1 | 19.10.20 | | |
| | Arithmetic pipeline | 1 | 21.10.20 | | |
| | Flynn's architecture | 1 | 2.11.20 | | |
| | **Assessment on this CHAPTER** | -- | | | Quiz |

## B. Daily Lesson Plan

| Lecture | TOPIC/UNIT/ CHAPTER | Plan date | Execution date | Details of home work/assignment/mini project/ICT used/other | Details of topics that are beyond syllabus (if any) | Remarks |
|---|---|---|---|---|---|---|
| 1. | Concept of basic components of a digital computer, Basic concept of Fundamentals & Program structures. Role of operating systems and compiler/assembler. | 16.7.20 | 17.8.20 | | | |
| 2. | Stored program concept, Von-Neumann architecture | 20.7.20 | 19.8.20 | | | |
| 3. | Basic number systems, Binary Arithmetic (Add, Sub, Mul, Div), Logic Gates, Boolean Algebra, BCD Addition, Binary Subtraction, 2's complement addition. | 22.7.20 | 20.8.20 | 1. Solve the following:<br>● 10101011+00111111=?<br>● 1000011+01010101=?<br>● 10001000-01101011 =?<br>● 00110011-00011100 =?<br>2. Prove the following using Boolean algebra operations: X'Y'Z'+ X'Y'Z + XY'Z = Y'(X'+Z)<br>3. Simplify the expression: X'Y'(X'+Y)(X'+X)<br>4. Verify: xy' + yz' + zx' = x'y + y'z + z'x<br>5. Solve:<br>a. $01011_2$ X $1001_2$<br>b. $111011_2$ / $111_2$ | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 4. | Concepts of Combinational Circuits: MUX, DEMUX, Decoder, Encoder, Sequential Circuit (Flip-Flop). | 23.7.20 | 21.8.20 | Design a 16: 1 MUX using 4:1 MUX.<br>Explain the differences between: MUX and DEMUX, Decoder and Encoder | | |
| 5. | Signed representation of Fixed point numbers. Arithmetic overflow. | 27.7.20 | 24.8.20 | 1. Represent the binary positive number 1101011 in floating point 32-bit IEEE format.<br>2. Represent the decimal number -0.75 in IEEE single precision format.<br><br>ASSIGNMENT* | | |
| 6. | Floating point representation of numbers (IEEE 754 standard), Overflow and underflow of floating point numbers. | 29.7.20 | 26.8.20 | ASSIGNMENT* | | |
| 7. | Fixed point multiplication -Booth's algorithm. | 30.7.20 | 27.8.20 | Multiply (-9 X 6) using Booth's algorithm.<br>Multiply (-3 X -12) using Booth's algorithm.<br><br>ASSIGNMENT* | | |
| 8. | Fixed point division - Restoring algorithms. | 3.8.20 | 31.8.20 | 3. Divide (6/3) using Restoring algorithm.<br>4. Divide (20/3) using Restoring algorithm. | | |
| 9. | Fixed point division -Non-restoring Algorithm | 5.8.20 | 2.9.20 | 1. Divide (15/5) using non-Restoring algorithm.<br>2. Divide (24/7) using non-Restoring algorithm. | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 10. | HA, FA, serial and parallel adders, Design of adders – Ripple carry adder, | 6.8.20 | 4.9.20 | | | |
| 11. | Carry look-ahead principles. | 10.8.20 | 7.9.20 | | | |
| 12. | Adder-Subtractor Unit, Binary Incrementer Unit, Decrementer Unit, | 12.8.20 | 9.9.20 | | | |
| 13. | Computer Registers. Bus (Data/ Address/ Control) | 13.8.20 | 11.9.20 | | | |
| 14. | Common Bus System | 17.8.20 | 14.9.20 | Construct a common bus system using 4:1 MUX for 4 registers. | | |
| 15. | Design of the Arithmetic and logic Unit of ALU | 19.8.20 | 16.9.20 | | | |
| 16. | Design of the shift Unit of ALU, Design of one stage of ALU | 20.8.20 | 18.9.20 | Design and explain one stage arithmetic logic shift unit of the ALU. | | |
| 17. | Memory Organization: Memory Hierarchy, Main Memory architecture, Implementation of CPU-memory interfacing, RAM and ROM chips. | 24.8.20 | 21.9.20 | | | |
| 18. | Types of RAM and ROM chips, classification of Secondary memory | 26.8.20 | 23.9.20 | | | |
| 19. | Memory address map | 27.8.20 | 25.9.20 | ASSIGNMENT* | | |
| 20. | Associative memory/ CAM: Cache memory | 31.8.20 | 28.9.20 | | | |
| 21. | Memory read/write cycle, avg. access time calculation | 2.9.20 | 29.9.20 | ASSIGNMENT* | | |
| 22. | Cache mapping techniques | 3.9.20 | 30.9.20 | | | |
| 23. | Cache mapping techniques | 7.9.20 | 5.10.20 | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | ASSIGNMENT* | | |
| 24. | Replacement methods, cache write methods, techniques to reduce cache miss | 9.9.20 | 7.10.20 | HOMEWORK | | |
| 25. | Virtual memory | 10.9.20 | 9.10.20 | | | |
| 26. | Basic Instruction format, Immediate, Direct address, Indirect address, Effective addresses. Instruction Formats : Memory/ Register/Input-Output reference. | 14.9.20 | 12.10.20 | | | |
| 27. | Types of Instruction: Data Transfer/ Data Manipulation/ Program Control | 16.9.20 | 13.10.20 | | | |
| 28. | Zero/One/Two/Three address instructions, RISC instructions. | 21.9.20 | 19.10.20 | 1. Represent x = (a + b) * c in Zero/One/Two/Three address and RISC instruction format.<br>2. Represent x = (a * b) / (c + d) in Zero/One/Two/Three address and RISC instruction format. | | |
| 29. | Introduction to RISC architectures, RISC vs. CISC architectures. | 24.9.20 | 2.11.20 | | | |
| 30. | Fetch, decode and execute cycle | 28.9.20 | 4.11.20 | | | |
| 31. | Design of control unit (CU) – hardwired and micro-programmed control | 1.10.20 | O9.11.20 | | | |
| 32. | Synchronous and Asynchronous data transfer, I/O operations - Concept of handshaking I/O | 5.10.20 | 10.11.20 | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 33. | Modes of data transfer: programmed I/O, interrupt driven I/O. | 7.10.20 | 11.11.20 | | | |
| 34. | Priority interrupt , Daisy chain, Polling | 8.10.20 | 15.12.20 | | | |
| 35. | Direct Memory Access (DMA) | 12.10.20 | 16.12.20 | | | |
| 36. | Pipelining | 14.10.20 | 5.1.21 | HOMEWORK | | |
| 37. | Hazards | 19.10.20 | 6.1.21 | | | |
| 38. | Arithmetic pipeline | 21.10.20 | 13.1.21 | | | |
| 39. | Flynn's architecture | 2.11.20 | 27.1.21 | | | |

*Details of Assignments are given later.

***ASSIGNMENTS**

**Computer Organization (PCC CS302)**

## ASSIGNMENT-1

**1.** Convert the following expressions into Zero/One/Two/Three address instructions, RISC instructions**:**

a. P = [(A*B+C)/(D+E*C)]

b. P = [{(A*B+C) – (D+B*C)}/(E*F)]

## ASSIGNMENT-2

1. Show the bus connection with a CPU to connect four RAM chips of size 256X8 bits each and a ROM chip of 512X8 bit size. Assume CPU has 8-bit data bus and 16-bit address bus. Clearly specify the generation of chip select signals.
2. Design a composite 1K×8 memory system using 256×2 RAM chips.
3. Design a composite 1K×8 memory system using two 256×8 RAM chips and two 256×8 ROM chips.
4. A magnetic disk pack has 12 surfaces out of which 10 are recordable. Each surface has 50 tracks and each track is divided into a number of sectors. The total capacity of the disk pack is 50000 K and capacity of each sector is 512 bytes.
   How many cylinders are present in the disk pack?
   How many sectors are present on each track?

## ASSIGNMENT-3

1. A hierarchical cache-main memory subsystem has the following specifications:

   · Cache access time of 160ns

   · Main memory access time of 960ns

   · Hit ratio of cache is 0.9

   Calculate the following:

   a. Average access time of the memory system

      i) Considering only read cycle.

      ii) Considering requests for both read and write.

   b. Efficiency of memory system.

2. A CPU has 32-bit memory address and a 256KB cache memory. The cache is organized as a 4-way set associative cache with cache block size of 16 bytes.

a. What is the number of sets in the cache?

b. What is the size (in bits) of the tag field per cache block?

c. What is the number of comparators required for tag matching (i.e. no. of bits required to identify different tag values)?

d. How many address bits are required for tag matching?

3. With the help of the following information, determine the size of the sub-fields (in bits) in the address for direct mapping, associative mapping and set-associative mapping:

- 512 MB main memory and 2 MB cache memory
- Address space of the processor is 256 MB
- The block size is 256 bytes
- There are 16 blocks in a cache set.

## (x) Teaching Strategy / Method

1) Taking interactive classes through different examples.
2) Conducting Question – answer session at the end of the class.
3) Real life application for better understanding.

## (xa) Strategy to support weak students

1) To engage the weak students in habit of studying, I give them some easy questions in regular basis.
2) Some weak students also have the problem of forgetting what they have learnt. In my class I always give some tips on how to recall and how to write systematically.
3) Weak students need special attention even after college hours. I always give some extra hours to weak students.

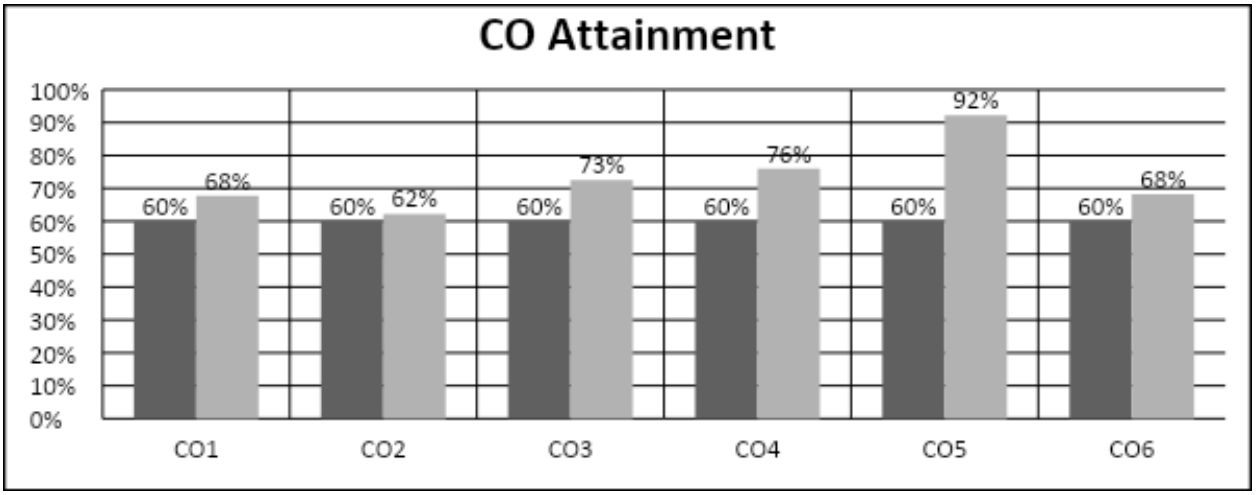
## (xb) Strategy to encourage bright students

1) Have an extra challenge ready that allows the student to go deeper into the subject, learn a little more, or apply a skill he has just learned in a new way.
2) Some students are engaged with the final year students for their final projects.

## (xc) Efforts to keep students engaged

**1)** Regular basis Home Work.
**2)** 5-10 minutes spent in an every class for question answer session.
**3)** Quiz on regular basis.
4) Some technical assignments are given group wise.

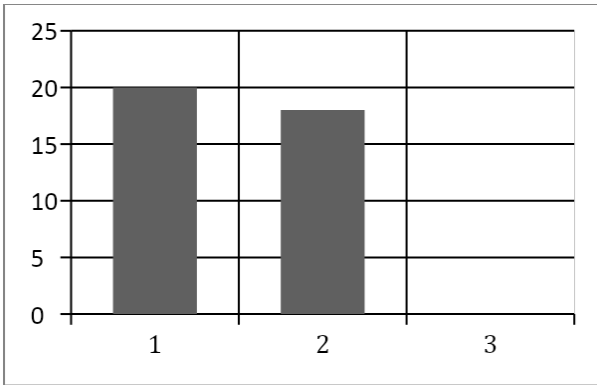
## (xi) Analysis of Students performance in the course

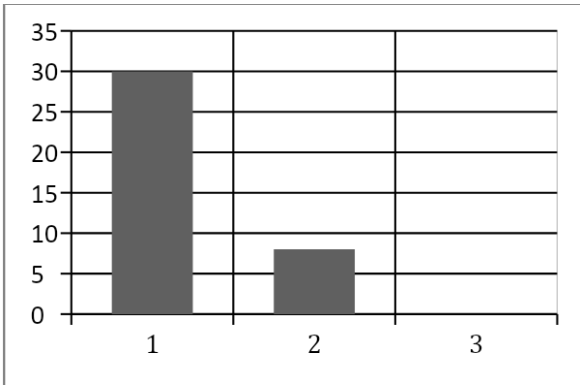


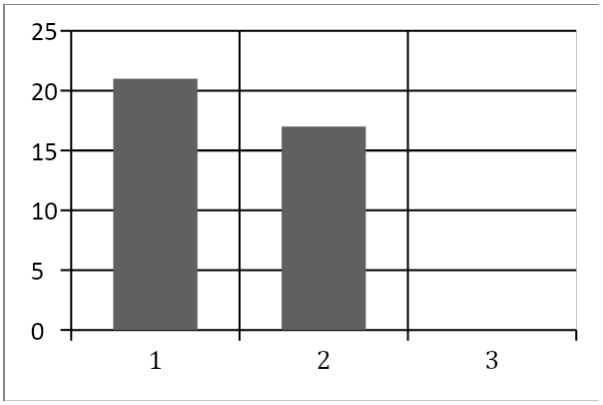
## (xii) Analysis of Students performance in the course (university results)

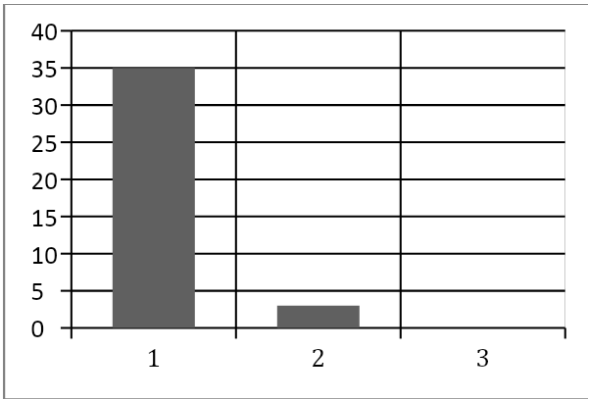
| | Target Course Outcome% | TOTAL STUDENTS | TOTAL STUDENT WHO ATTAINED OUTCOME | % STUDENTS WHO ATTAINED THE OUTCOME |
|---|---|---|---|---|
| University Result | 60% | 45 | 44 | 98 |

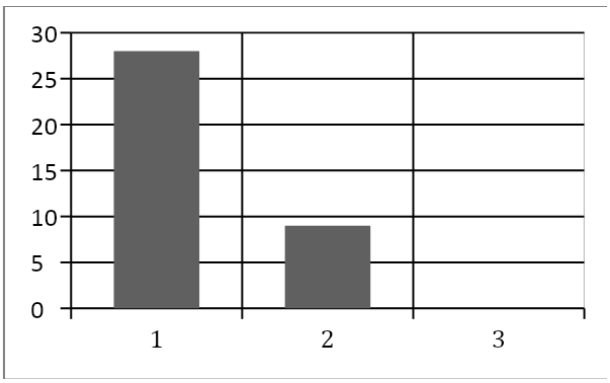
## (xiii) Analysis of Student Feed Back

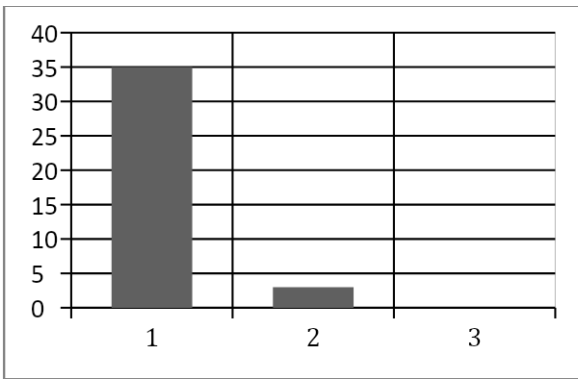





## (xiv) Teacher Self-Assessment (at the completion of course)

From the analysis of the results obtained it can be seen that set targets for the course outcome have been achieved successfully by the students. Since this subject is a pre-requisite for Advanced Computer Architecture in 4$^{th}$ semester, more emphasis must be given for Parallel processing and pipelining.

## (xiv) Recommendations/Suggestions for improvement by faculty

- More emphasis should be given to clear the concepts of Memory Unit.
- Tutorials must be incorporated in the syllabus.
- Increase the total contact hours for theory to 40 hrs, with 4L per week.

| Sl. | Roll No. | Name | Attendance | | Internal Examination | | | Assignment / Quiz |
|---|---|---|---|---|---|---|---|---|
| | | | Total | Marks | 1st | 2nd | Avg. | |
| 1 | 11900119004 | SEEMA NITISH RAO | 75 | 3 | 16 | 25 | 20.5 | 6 |
| 2 | 11900119005 | RAJ KISHOR PRASAD | 83 | 4 | 21 | 28 | 24.5 | 9 |
| 3 | 11900119006 | RAGHAV SOMANI | 78 | 3 | 22 | 27 | 24.5 | 9 |
| 4 | 11900119007 | MD AAMIR SHEKH | 99 | 5 | 27 | 24 | 25.5 | 10 |
| 5 | 11900119008 | KARAN SHARMA | 79 | 3 | 23 | 26 | 24.5 | 8 |
| 6 | 11900119009 | MOHAMMED SAHIL | 79 | 3 | 20 | 24 | 22 | 10 |
| 7 | 11900119010 | JAMIL AKHTAR LASKAR | 86 | 4 | 22 | 23 | 22.5 | 7 |
| 8 | 11900119011 | PAWAN KUMAR GUPTA | 93 | 5 | 17 | 25 | 21 | 8 |
| 9 | 11900119012 | DIPTARKA BHATTACHARYA | 91 | 5 | 18 | 23 | 20.5 | 7 |
| 10 | 11900119013 | NIVEDITA PRASAD | 75 | 3 | 18 | 23 | 20.5 | 8 |
| 11 | 11900119014 | ANIKET DEB | 98 | 5 | 28 | 24 | 26 | 10 |
| 12 | 11900119015 | DEEP DHAR | 79 | 3 | 19 | 25 | 22 | 7 |
| 13 | 11900119016 | HARSH KUMAR | 86 | 4 | 20 | 22 | 21 | 10 |
| 14 | 11900119017 | ANIKET DASGUPTA | | | | | | |
| 15 | 11900119018 | RAHUL KUMAR | 98 | 5 | 20 | 23 | 21.5 | 10 |
| 16 | 11900119019 | NILASISH MOHANTI | 95 | 5 | 14 | 25 | 19.5 | 10 |
| 17 | 11900119020 | MD SHOAIB AKHTAR | 91 | 5 | 15 | 25 | 20 | 10 |
| 18 | 11900119021 | AMARTYA SARKAR | 79 | 3 | 17 | 25 | 21 | 8 |
| 19 | 11900119022 | ARKA ROY CHOUDHURY | 84 | 4 | 15 | 26 | 20.5 | 8 |
| 20 | 11900119023 | PARTHIB BOSE | 81 | 4 | 14 | 23 | 18.5 | 9 |
| 21 | 11900119024 | PARAMHANS SHAH | 93 | 5 | 24 | 25 | 24.5 | 10 |
| 22 | 11900119025 | SUVADITYA GUPTA | 84 | 4 | 28 | 27 | 27.5 | 10 |
| 23 | 11900119026 | NAUSHAD ALAM | 79 | 3 | 24 | 28 | 26 | 5 |
| 24 | 11900119027 | CHIRAG AGARWALLA | 93 | 5 | 16 | 28 | 22 | 9 |
| 25 | 11900119028 | Purabi Ghosh | 91 | 5 | 28 | 22 | 25 | 9 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 26 | 11900119029 | DEBARGHA DEY | 76 | 3 | 27 | 23 | 25 | 9 |
| 27 | 11900119030 | DEBARKO GHOSH | 84 | 4 | 23 | 27 | 25 | 7 |
| 28 | 11900119031 | FALGUNI SARKAR | 81 | 4 | 15 | 26 | 20.5 | 9 |
| 29 | 11900119032 | ALOK KUMAR SAH | 93 | 5 | 25 | 24 | 24.5 | 9 |
| 30 | 11900119033 | SAMARPAN GHOSH | 91 | 5 | 22 | 26 | 24 | 10 |
| 31 | 11900119034 | SOUMEN SARKAR | 98 | 5 | 23 | 22 | 22.5 | 9 |
| 32 | 11900119035 | SHIBABRATA BOSE | 86 | 4 | 24 | 28 | 26 | 7 |
| 33 | 11900119036 | ABIR PAUL | 91 | 5 | 15 | 25 | 20 | 10 |
| 34 | 11900119037 | SHANKHYA JYOTI DHAR | 84 | 4 | 22 | 27 | 24.5 | 7 |
| 35 | 11900119038 | BARNALI BASAK | 81 | 4 | 22 | 26 | 24 | 9 |
| 36 | 11900119039 | VED PRAKASH BHASKAR | 84 | 4 | 22 | 22 | 22 | 7 |
| 37 | 11900119040 | ARITRA KUMAR DATTA CHAUDHURY | 81 | 4 | 28 | 23 | 25.5 | 9 |
| 38 | 11900119041 | ABIJIT CHETTRI | 88 | 4 | 19 | 25 | 22 | 8 |
| 39 | 11900119042 | SUPRAKASH MAITY | 86 | 4 | 15 | 23 | 19 | 9 |
| 40 | 11900119043 | ANKIT ANAND | 91 | 5 | 28 | 25 | 26.5 | 9 |
| 41 | 11900119044 | ABHISHEK SUMAN | 76 | 3 | 23 | 22 | 22.5 | 7 |
| 42 | 11900119045 | ANURAG DAS | 84 | 4 | 24 | 26 | 25 | 10 |
| 43 | 11900119046 | GOVINDA DARSHAN | 81 | 4 | 22 | 25 | 23.5 | 7 |
| 44 | 11900119047 | SAYANI GHOSH | 93 | 5 | 27 | 23 | 25 | 9 |
| 45 | 11900119048 | SUMIT MAN | 91 | 5 | 20 | 22 | 21 | 8 |

# LIST OF PRACTICALS

**Subject with code:_____ Section:____**

**Semester :_____ Discipline:_____**

| Sl. | Details of Experiment(s) | Hours allotted |
|---|---|---|
| P1 | Familiarization with IC chips:<br>a) 4:1 MUX,<br>b) 16:1 MUX<br>c) Decoder<br>d) Encoder<br>e) Comparator<br><br>Truth table verification and clarification from data-book. | 7 HRS |
| P2 | Design of Adder/Subtractor composite unit | 2 HRS |
| P3 | Design of BCD Adder | 2 HRS |
| P4 | Design of Carry Look-Ahead Adder | 3 HRS |
| P5 | Use a multiplexer unit to design a composite ALU | 3 HRS |
| P6 | Use ALU chip for multi-bit arithmetic operation | 3 HRS |
| P7 | Implement read/write operation using RAM IC | 3 HRS |
| P8 | Cascade two ICs for<br>a) vertical expansion<br>b) horizontal expansion | 3 HRS |
| | | |
| | | |

| Sl | Roll No. | Name | Marks in experimentation | | | | | | | | | | Total |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | E1 | E2 | E3 | E4 | E5 | E6 | E7 | E8 | | | |
| | | | 15 | 4 | 4 | 3 | 4 | 3 | 4 | 3 | | | |
| 1 | 11900119004 | SEEMA NITISH RAO | 13 | 4 | 4 | 2 | 3 | 3 | 4 | 3 | | | **36** |
| 2 | 11900119005 | RAJ KISHOR PRASAD | 14 | 4 | 4 | 2 | 4 | 3 | 4 | 3 | | | **38** |
| 3 | 11900119006 | RAGHAV SOMANI | 13 | 4 | 3 | 2 | 3 | 3 | 4 | 4 | | | **36** |
| 4 | 11900119007 | MD AAMIR SHEKH | 13 | 4 | 3 | 1 | 4 | 3 | 3 | 4 | | | **35** |
| 5 | 11900119008 | KARAN SHARMA | 12 | 3 | 3 | 1 | 4 | 3 | 3 | 3 | | | **32** |
| 6 | 11900119009 | MOHAMMED SAHIL | 13 | 3 | 3 | 1 | 3 | 2 | 4 | 3 | | | **32** |
| 7 | 11900119010 | JAMIL AKHTAR LASKAR | 14 | 4 | 4 | 1 | 4 | 3 | 4 | 3 | | | **37** |
| 8 | 11900119011 | PAWAN KUMAR GUPTA | 13 | 4 | 4 | 2 | 3 | 3 | 4 | 3 | | | **36** |
| 9 | 11900119012 | DIPTARKA BHATTACHARYA | 15 | 4 | 3 | 2 | 4 | 3 | 4 | 3 | | | **38** |
| 10 | 11900119013 | NIVEDITA PRASAD | 15 | 4 | 4 | 2 | 4 | 3 | 4 | 3 | | | **39** |
| 11 | 11900119014 | ANIKET DEB | 14 | 4 | 3 | 3 | 4 | 3 | 4 | 3 | | | **38** |
| 12 | 11900119015 | DEEP DHAR | 12 | 3 | 3 | 1 | 4 | 2 | 3 | 2 | | | **30** |
| 13 | 11900119016 | HARSH KUMAR | 14 | 4 | 4 | 2 | 3 | 3 | 4 | 3 | | | **37** |
| 14 | 11900119017 | ANIKET DASGUPTA (LEFT) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | **0** |
| 15 | 11900119018 | RAHUL KUMAR | 13 | 4 | 4 | 1 | 3 | 3 | 4 | 3 | | | **35** |
| 16 | 11900119019 | NILASISH MOHANTI | 14 | 4 | 3 | 2 | 3 | 3 | 4 | 3 | | | **36** |
| 17 | 11900119020 | MD SHOAIB AKHTAR | 14 | 4 | 4 | 1 | 4 | 3 | 4 | 3 | | | **37** |
| 18 | 11900119021 | AMARTYA SARKAR | 14 | 4 | 3 | 2 | 4 | 3 | 4 | 3 | | | **37** |
| 19 | 11900119022 | ARKA ROY CHOUDHURY | 14 | 4 | 4 | 1 | 4 | 3 | 4 | 3 | | | **37** |
| 20 | 11900119023 | PARTHIB BOSE | 13 | 4 | 4 | 2 | 3 | 3 | 4 | 3 | | | **36** |
| 21 | 11900119024 | PARAMHANS SHAH | 13 | 4 | 4 | 2 | 3 | 3 | 4 | 3 | | | **36** |
| 22 | 11900119025 | SUVADITYA GUPTA | 14 | 4 | 4 | 1 | 4 | 3 | 3 | 4 | | | **37** |
| 23 | 11900119026 | NAUSHAD ALAM | 14 | 4 | 4 | 1 | 4 | 3 | 3 | 3 | | | **36** |
| 24 | 11900119027 | CHIRAG AGARWALLA | 13 | 4 | 4 | 1 | 4 | 3 | 4 | 3 | | | **36** |

| Sl | Roll No. | Name | Marks in experimentation | | | | | | | | | | Total |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
| | | | 15 | 4 | 4 | 3 | 4 | 3 | 4 | 3 | | | |
| 25 | 11900119028 | Purabi Ghosh | 12 | 4 | 4 | 1 | 4 | 2 | 4 | 3 | | | **34** |
| 26 | 11900119029 | DEBARGHA DEY | 12 | 4 | 3 | 1 | 3 | 2 | 3 | 2 | | | **30** |
| 27 | 11900119030 | DEBARKO GHOSH | 13 | 3 | 3 | 1 | 3 | 2 | 4 | 3 | | | **32** |
| 28 | 11900119031 | FALGUNI SARKAR | 13 | 4 | 4 | 1 | 3 | 3 | 4 | 3 | | | **35** |
| 29 | 11900119032 | ALOK KUMAR SAH | 14 | 4 | 3 | 2 | 4 | 3 | 4 | 3 | | | **37** |
| 30 | 11900119033 | SAMARPAN GHOSH | 13 | 4 | 4 | 1 | 3 | 3 | 4 | 3 | | | **35** |
| 31 | 11900119034 | SOUMEN SARKAR | 15 | 4 | 4 | 2 | 4 | 3 | 4 | 3 | | | **39** |
| 32 | 11900119035 | SHIBABRATA BOSE | 13 | 4 | 4 | 2 | 3 | 3 | 4 | 3 | | | **36** |
| 33 | 11900119036 | ABIR PAUL | 13 | 4 | 4 | 1 | 3 | 3 | 4 | 3 | | | **35** |
| 34 | 11900119037 | SHANKHYA JYOTI DHAR | 12 | 4 | 3 | 1 | 4 | 3 | 3 | 3 | | | **33** |
| 35 | 11900119038 | BARNALI BASAK | 13 | 4 | 3 | 1 | 3 | 2 | 4 | 3 | | | **33** |
| 36 | 11900119039 | VED PRAKASH BHASKAR | 14 | 3 | 3 | 1 | 4 | 3 | 4 | 1 | | | **35** |
| 37 | 11900119040 | ARITRA KUMAR DATTA CHAUDHURY | 13 | 3 | 3 | 1 | 4 | 3 | 3 | 3 | | | **33** |
| 38 | 11900119041 | ABIJIT CHETTRI | 13 | 3 | 3 | 1 | 3 | 3 | 4 | 3 | | | **33** |
| 39 | 11900119042 | SUPRAKASH MAITY | 12 | 3 | 3 | 1 | 4 | 3 | 3 | 3 | | | **32** |
| 40 | 11900119043 | ANKIT ANAND | 12 | 3 | 3 | 1 | 4 | 2 | 3 | 2 | | | **30** |
| 41 | 11900119044 | ABHISHEK SUMAN | 12 | 3 | 2 | 1 | 0 | 1 | 2 | 1 | | | **22** |
| 42 | 11900119045 | ANURAG DAS | 12 | 3 | 3 | 1 | 4 | 2 | 3 | 2 | | | **30** |
| 43 | 11900119046 | GOVINDA DARSHAN | 14 | 4 | 4 | 2 | 3 | 3 | 4 | 3 | | | **37** |
| 44 | 11900119047 | SAYANI GHOSH | 13 | 4 | 3 | 1 | 4 | 3 | 4 | 3 | | | **35** |
| 45 | 11900119048 | SUMIT MAN | 13 | 4 | 4 | 1 | 3 | 3 | 4 | 3 | | | **35** |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |

**RECORDS OF ASSIGNMENTS/~~QUIZ~~**

**Paper Name: COMPUTER ORGANIZATION**

**Paper Code: CS 601**

| Sl. | Roll No. | Name | A1 | A2 | A3 | Sl. | Roll No. | Name | A1 | A2 | A3 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 11900119004 | SEEMA NITISH RAO | 1 | 0 | 1 | 25 | 11900119028 | Purabi Ghosh | 1 | 1 | 1 |
| 2 | 11900119005 | RAJ KISHOR PRASAD | 1 | 1 | 1 | 26 | 11900119029 | DEBARGHA DEY | 1 | 1 | 1 |
| 3 | 11900119006 | RAGHAV SOMANI | 1 | 1 | 1 | 27 | 11900119030 | DEBARKO GHOSH | 1 | 1 | 1 |
| 4 | 11900119007 | MD AAMIR SHEKH | 1 | 1 | 1 | 28 | 11900119031 | FALGUNI SARKAR | 1 | 1 | 1 |
| 5 | 11900119008 | KARAN SHARMA | 1 | 1 | 1 | 29 | 11900119032 | ALOK KUMAR SAH | 1 | 1 | 1 |
| 6 | 11900119009 | MOHAMMED SAHIL | 1 | 1 | 1 | 30 | 11900119033 | SAMARPAN GHOSH | 1 | 1 | 1 |
| 7 | 11900119010 | JAMIL AKHTAR LASKAR | 1 | 1 | 1 | 31 | 11900119034 | SOUMEN SARKAR | 1 | 1 | 1 |
| 8 | 11900119011 | PAWAN KUMAR GUPTA | 1 | 1 | 1 | 32 | 11900119035 | SHIBABRATA BOSE | 1 | 1 | 1 |
| 9 | 11900119012 | DIPTARKA BHATTACHARYA | 1 | 1 | 1 | 33 | 11900119036 | ABIR PAUL | 1 | 1 | 1 |
| 10 | 11900119013 | NIVEDITA PRASAD | 1 | 1 | 1 | 34 | 11900119037 | SHANKHYA JYOTI DHAR | 1 | 1 | 1 |
| 11 | 11900119014 | ANIKET DEB | 1 | 1 | 1 | 35 | 11900119038 | BARNALI BASAK | 1 | 1 | 1 |
| 12 | 11900119015 | DEEP DHAR | 1 | 1 | 1 | 36 | 11900119039 | VED PRAKASH BHASKAR | 1 | 1 | 1 |
| 13 | 11900119016 | HARSH KUMAR | 1 | 1 | 1 | 37 | 11900119040 | ARITRA KUMAR DATTA CHAUDHURY | 1 | 1 | 1 |
| 14 | 11900119017 | ANIKET DASGUPTA (LEFT) | 0 | 0 | 0 | 38 | 11900119041 | ABIJIT CHETTRI | 1 | 1 | 1 |
| 15 | 11900119018 | RAHUL KUMAR | 1 | 1 | 1 | 39 | 11900119042 | SUPRAKASH MAITY | 1 | 1 | 1 |
| 16 | 11900119019 | NILASISH MOHANTI | 1 | 1 | 1 | 40 | 11900119043 | ANKIT ANAND | 1 | 1 | 1 |
| 17 | 11900119020 | MD SHOAIB AKHTAR | 1 | 1 | 1 | 41 | 11900119044 | ABHISHEK SUMAN | 1 | 1 | 1 |
| 18 | 11900119021 | AMARTYA SARKAR | 1 | 1 | 1 | 42 | 11900119045 | ANURAG DAS | 0 | 1 | 1 |
| 19 | 11900119022 | ARKA ROY CHOUDHURY | 1 | 1 | 1 | 43 | 11900119046 | GOVINDA DARSHAN | 1 | 1 | 1 |
| 20 | 11900119023 | PARTHIB BOSE | 1 | 1 | 1 | 44 | 11900119047 | SAYANI GHOSH | 1 | 1 | 1 |
| 21 | 11900119024 | PARAMHANS SHAH | 1 | 1 | 1 | 45 | 11900119048 | SUMIT MAN | 1 | 1 | 1 |
| 22 | 11900119025 | SUVADITYA GUPTA | 1 | 1 | 1 | | | | | | |
| 23 | 11900119026 | NAUSHAD ALAM | 0 | 1 | 1 | | | | | | |
| 24 | 11900119027 | CHIRAG AGARWALLA | 1 | 1 | 1 | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |

| NAME WITH ROLL NO.s OF STUDENT WHOSE ACADEMIC PERFOMANCE IS NOT SATISFACTORY | | | |
|---|---|---|---|
| **Sl.** | **Roll No.** | **Name of Student** | **Remedial measures taken by teacher** |
| 1 | 11900119004 | SEEMA NITISH RAO | Discussions held on doubt clearing class related to the subject contents |
| 2 | | | |
| 3 | | | |
| 4 | | | |
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# CERTIFICATE

I, the undersigned, have completed the course allotted to me as shown below

| Sl. No. | Semester | Subject with Code | Total Units/ Chapters | Remarks |
|---|---|---|---|---|
| | | | | |

| | |
|---|---|
| Date : | **Signature of Faculty** |

**Submitted to HOD**

Certificate by HOD

I, the undersigned, certify that……..has completed the course work allotted to him/ her satisfactorily/ not satisfactorily.

| | |
|---|---|
| Date : | **Signature of HOD** |

**Submitted to Principal/Director**

| | |
|---|---|
| Date : | **Signature of Principal/Director** |